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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,728	12/02/2005	Yukio Sakashita	123887	7173

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EXAMINER	
THOMAS, ERIC W	
ART UNIT	PAPER NUMBER
2831	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,728	SAKASHITA ET AL.	
	Examiner	Art Unit	
	Eric Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/25/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *3,6-8 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-5, 9, 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/12/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/08, 6/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Information Disclosure Statement

1. The information disclosure statement filed 6/25/08 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

3. Claim 1 recites the limitation "the formula $Bi_2A_{2-x}RexB_3O_{12}$" in line 15. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 1 recites the limitation "the formula $Bi_2A_{3-x}RexB_4O_{15}$" in line 16. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-2, 4-5, 11, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. (JP 2001-144263) in view of Nabatame et al. (US 6,198,119) and JP 2001-326305 ('305).

Hashimoto et al. disclose a thin film capacitor device comprising a dielectric thin film, wherein said dielectric thin film is comprised of a bismuth layer structured compound, said bismuth layer structured compound is expressed by the formula $(Bi_2O_2)^{2+}$ $(A_{m-1}B_mO_{3m+1})^{2-}$ (see paragraph 29), where m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W, said dielectric thin film further includes at least one rare earth element Re selected from Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm,

Yb and Lu (paragraph 29 - A is at least one selected from Bi, Pb, Ba, Sr, Ca, Na, K and a rare earth element).

Hashimoto et al. disclose the claimed invention except that the bismuth layer structure compound has a c-axis oriented vertically to the substrate surface.

Nabatame et al. disclose a bismuth layer structure compound having a c-axis that is oriented vertically to a substrate surface.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the bismuth layer of the device of Hashimoto by forming the layer with its c-axis oriented vertically to the substrate surface as taught by Nabatame, since such a modification would from a planar capacitor device having large spontaneous polarization.

Hashimoto et al. disclose the claimed invention except that the device is a thin film capacitor for reducing power noise connected to a power source.

‘305 discloses a thin film capacitor for reducing power noise connected to a power source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the dielectric material of Nabatame in the capacitor of ‘305, since such a modification would form a capacitor having a bismuth layer structure compound insulator having a high dielectric constant.

Regarding claim 2, ‘305 discloses the capacitor is a decoupling capacitor connected in parallel between the power source and an integrated circuit.

Regarding claim 4, '305 discloses the capacitor is arranged near an integrated circuit chip.

Regarding claim 5, '305 discloses the capacitor is arranged in contact with an integrated circuit.

Regarding claim 11, '305 disclose the capacitor has a lower electrode formed on a thin film substrate, the dielectric thin film formed on said lower electrode, and an upper electrode formed on said dielectric thin film (see fig. 6).

Regarding claim 13, the modified Hashimoto et al. disclose that the bismuth layer structure compound has a c axis orientation of at least 80%.

8. Claims 1-2, 9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. (JP 2001-144263) in view of Nabatame et al. (US 6,198,119), Iino et al. (US 6,370,013) and Takeshima et al. (JP 11-214245).

Regarding claims 1, 2, 9, and 12, Hashimoto et al. disclose a thin film capacitor device comprising a dielectric thin film, wherein said dielectric thin film is comprised of a bismuth layer structured compound, said bismuth layer structured compound is expressed by the formula $(Bi_2O_2)^{2+}$ $(A_{m-1}B_mO_{3m+1})^{2-}$ (see paragraph 29), where m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W, said dielectric thin film further includes at least one rare earth element Re selected from Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu.

Hashimoto et al. disclose the claimed invention except that the bismuth layer structure compound has a c-axis oriented vertically to the substrate surface.

Nabatame et al. disclose a bismuth layer structure compound having a c-axis that is oriented vertically to a substrate surface.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the bismuth layer of the device of Hashimoto by forming the layer with its c-axis oriented vertically to the substrate surface as taught by Nabatame, since such a modification would from a planar capacitor device having large spontaneous polarization.

Hashimoto et al. disclose the claimed invention except that the device is a thin film monolithic capacitor comprising electrodes separated by dielectric layers.

Takeshima et al. disclose a thin film monolithic capacitor comprising electrodes separated by dielectric layers.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the dielectric material of the modified Hashimoto et al. in the monolithic capacitor of Takeshima et al., since such a modification would form a capacitor with a bismuth layer structure compound insulator having a high dielectric constant.

The modified Hashimoto et al disclose the claimed invention except that the capacitor functions as a decoupling capacitor within a printed circuit board.

Iino et al. teach that it is known in the art to connect a monolithic thin film capacitor between a power source and an integrated circuit so as to reduce the power source noise.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the monolithic capacitor of modified Hashimoto et al. in the printed circuit board of Iino et al., since such a modification would form a thin stacked type capacitor within a printed circuit board, wherein the thin stacked type capacitor has a high dielectric constant insulator.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-2, 4-5, 11-13 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 of U.S. Patent No. 7,145,198 ('198) in view of JP 2001-326305 ('305).

Regarding claim 1, '198 discloses a dielectric thin film comprised of a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, said bismuth layer structured compound is expressed by the formula $Bi_2A_{2-x}Re_xB_3O_{12}$, where the symbol m in said formula is 3, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W, said dielectric thin film further includes at least one rare earth element Re selected from Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu, and an amount of substitution by the rare earth element Re, X, is in the range of (i) $0.4 \leq X \leq 1.8$ (see claim 1).

'198 discloses the claimed invention except that the device is a thin film capacitor for reducing power noise connected to a power source.

'305 discloses a thin film capacitor for reducing power noise connected to a power source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the dielectric material of '198 in the capacitor of '305, since such a modification would form a capacitor having a bismuth layer structure compound insulator having a high dielectric constant.

Regarding claim 2, '305 discloses the capacitor is a decoupling capacitor connected in parallel between the power source and an integrated circuit.

Regarding claim 4, '305 discloses the capacitor is arranged near an integrated circuit chip.

Regarding claim 5, '305 discloses the capacitor is arranged in contact with an integrated circuit.

Regarding claim 11, '305 disclose the capacitor has a lower electrode formed on a thin film substrate, the dielectric thin film formed on said lower electrode, and an upper electrode formed on said dielectric thin film (see fig. 6).

Regarding claim 13, '198 discloses that the bismuth layer structure compound has a c axis orientation of at least 80% (claim 2).

11. Claims 1, 2, 9, and 12 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,145,198 ('198) in view of Iino et al. (US 6,370,013) and Takeshima et al. (JP 11-214245).

Regarding claims 1, 2, 9, and 12, '198 discloses a dielectric thin film comprised of a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, said bismuth layer structured compound is expressed by the formula $Bi_2A_{2-x}Re_xB_3O_{12}$, where the symbol m in said formula is 3, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W, said dielectric thin film further includes at least one rare earth element Re selected from Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu, and an amount of substitution by the rare earth element Re, X, is in the range of (i) $0.4 \leq X \leq 1.8$ (see claim 1).

'198 discloses the claimed invention except that the device is a thin film monolithic capacitor comprising electrodes separated by dielectric layers.

Takeshima et al. disclose a thin film monolithic capacitor comprising electrodes separated by dielectric layers.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the dielectric material of '198 in the monolithic capacitor of Takeshima et al., since such a modification would form a capacitor with a bismuth layer structure compound insulator having a high dielectric constant.

The modified '198 discloses the claimed invention except that the capacitor functions as a decoupling capacitor within a printed circuit board.

Iino et al. teach that it is known in the art to connect a monolithic thin film capacitor between a power source and an integrated circuit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the monolithic capacitor of modified '198 in the printed circuit board of Iino et al., since such a modification would form a thin stacked type capacitor within a printed circuit board, wherein the thin stacked type capacitor has a high dielectric constant insulator.

Response to Arguments

12. Applicant's arguments with respect to claims 1-2, 4-5, 9 and 11-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Translation of paragraph 29 - Hashimoto et al. (JP 2001-144263)

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on Monday - Friday 5:30 AM - 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eric Thomas/
Primary Examiner, Art Unit 2831